

1.General Specifications

Operating Temp.	:	min. 0°C ~max. 50°C
Storage Temp.	:	min. -20°C ~max. 70°C
Outline Dimensions	:	57.28 (W) × 47.74* (H) × 1.9 (D) mm * Without FPC and Area of Injection Port
Active Viewing Area	:	49.20(W) × 38.14(H) mm (2.5inch diagonal)
Resolution	:	480(W) × 234 (H) dots
Dot Pitch	:	0.103 (W) × 0.163(H)
Weight	:	17g
LCD type	:	Transmissive TFT-LCD/normally white
Viewing Angle	:	6:00
Interface	:	Compatible with NTSC or PAL system Analog RGB interface
Lighting	:	None
Drawing	:	Mechanical Outline UE-312295
Lead free	:	Our product corresponds to lead free. Lead free is defined as below: The solder used in the LCD module. Electrical components (Terminal section) used in the LCD module. Any lead used within the electrical component does not apply to our module definition of lead free.

2. Electrical Specifications

2.1. Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

GND=0V, Ta=25°C

Parameter	Symbol	MIN.	MAX.	Unit	Remark	
Supply Voltage For Source Driver	Analog	AV_{DD}	-0.3	+7.0	V	
	Digital	V_{DD}	-0.3	+7.0		
Supply Voltage For Gate Driver	Positive	V_{GH}	-0.3	+45	V	
	Negative	V_{GL}	-23	+0.3	V	
		$V_{GH} V_{GL}$	+15	+40	V	
Analog input voltage	V_{Video}	-0.3	+7.3	V	Note 2-1	
Storage Temperature		-20	+70	°C		
Operation Temperature		0	+50	°C	Note 2-2	

Note 2-1: Analog Input Voltage means V_R, V_G, V_B .

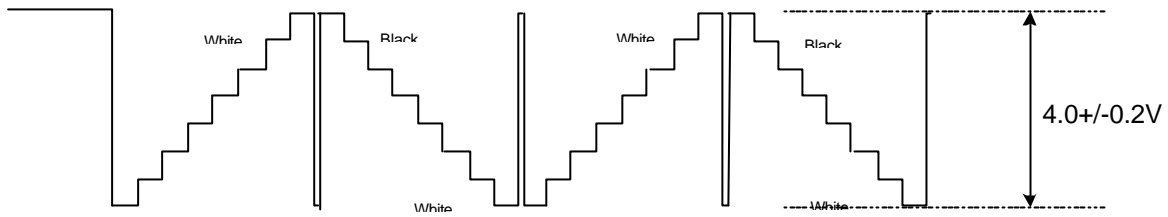
Note 2-2: Operating Temperature define that contrast, response time, other display optical character are Ta=+25°C.

2.2. Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply	V_{DD}	+4.5	+5.0	+5.5	V	
		+2.7	+3.3	+3.6		
	AV_{DD}	+4.5	+5.0	+5.5	V	
	V_{GH}	+14.5	+15.0	+15.5	V	
	V_{GLAC}	-	+6.0	-	V_{P-P}	AC Component of V_{GL}
	V_{GLDC}	-13.0	-12.5	-12.0	V	DC Component of V_{GL}
Video Signal (V_R, V_G, V_B)	V_{iAC}	-	+4.0	+4.2	V_{P-P}	AC Component Note 2-4
	V_{iDC}	-	+2.5	-	V	DC Component
V_{COM}	V_{COMAC}	-	+5.0	-	V_{P-P}	AC Component of V_{COM}
	V_{COMDC}	+1.24	+1.37	+1.50	V	DC Component of V_{COM}
H Level	V_{IH}	+0.7 V_{DD}	-	-	V	Note 2-3
	V_{IL}	-	-	+0.3 V_{DD}	V	

Note 2-3 : STH1, STH2, CPH1, CPH2, CPH3, Q2H, INH, CPV, XOE, DIO1, DIO2

Note 2-4: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



2.3. Current Consumption (GND=AV_{SS}=0V)

Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for Driver Black	I _{GH}	V _{GH} =+15V	-	0.026	0.03	mA	
	I _{GL}	V _{GL} =-12V	-	0.35	0.4	mA	V _{GL} center voltage
	I _{CC}	V _{CC} =+5V	-	0.1	0.15	mA	
	A _{DD}	AV _{DD} =+5V	-	1.73	1.83	mA	
	I _{DD}	V _{DD} =+5V	-	0.66	0.7	mA	

2.4. Power Consumption

Ta=25°C

Parameter	Symbol	Conditions	TYP.	Unit	Remark
LCD Panel Power Consumption			(25.0)	mW	

2.5. Input / Output Connector

LCD Module Connector
 FPC Down Connector
 24 Pins
 Pitch:0.5 mm

2.6. Timing Characteristics of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
1Field Scanning Period	t1V	-	262.5	-	H	
1Line Scanning Period	t1H	-	63.5	-	μs	
Source Driver Operating Frequency	f _{hc}	1.0	3.14	5.0	MHz	
Signal Sampling Pulse Width	t _{chw}	200	317.7	1000	ns	
Signal Sampling Pulse Delay	t _{chd}	95.3	105.9	116.5	ns	t _{chd} 12,23
Signal Sampling Pulse Width(H)	t _{chwh}	142.9	158.8	174.7	ns	
Signal Sampling Pulse Delay(L)	t _{chwl}	142.9	158.8	174.7	ns	
Source Start Signal Pulse Width	t _{shw}	90	317.7	630*	ns	*t _{shset} =t _{sh}
Source Start Signal Setup Time	t _{shset}	20	158.8	-	ns	
Source Start Signal Hold Time	t _{shhld}	20	158.8	-	ns	
Source Output Enable Pulse Width	t _{ohw}	1.0	2.0	-	μs	
Source Start Signal Rising Time	t _{ss}	-	9.8	-	μs	
Video Input Signal Start Point	t _{vs}	-	10.0	-	μs	
Phase Difference Between OEH&CPV	t _{oc}	1.5	2.3	-	μs	
Gate Clock Period	t _{cvw}	10	63.5	-	μs	
Gate Clock Pulse Width(H)	t _{cvwh}	10	31.7	48	μs	
Gate Clock Pulse Width(L)	t _{cvwl}	10	31.7	48	μs	
Gate Start Signal Pulse Width	t _{sw}	5	63.5	126**	μs	**t _{svset} =t _{sv}
Gate Start Signal Setup Time	t _{svset}	5	53.2	-	μs	
Gate Start Signal Hold Time	t _{svhld}	5	10.3	-	μs	
Phase Difference Between INH&STH	t _{osp}	-	4	-	μs	
Phase Difference Between SYNC&INH	t _{ohs}	-	1.4	-	μs	
Gate Output Enable Pulse Width	t _{oev}	-	2.5	-	μs	
V _{COM} Delay Time	t _{DCOM}	-	-	3	μs	
RGB Delay Time	t _{DRGB}	-	-	2	μs	
Vertical Display Start	t _{sv}	-	3	-	tH	

2.7. Signal Timing Waveforms

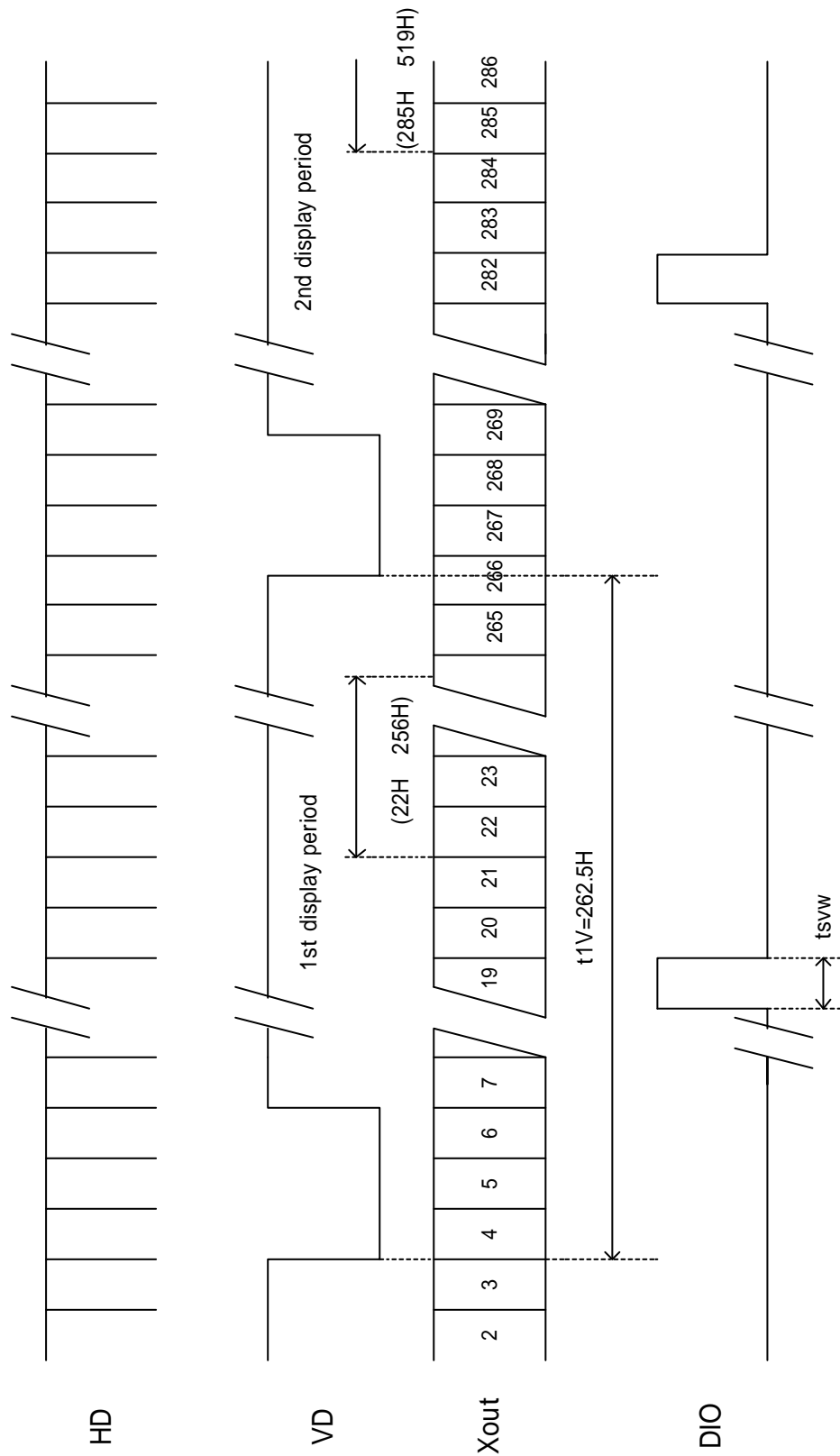


Fig. 2-1 Vertical Start Line for NTSC

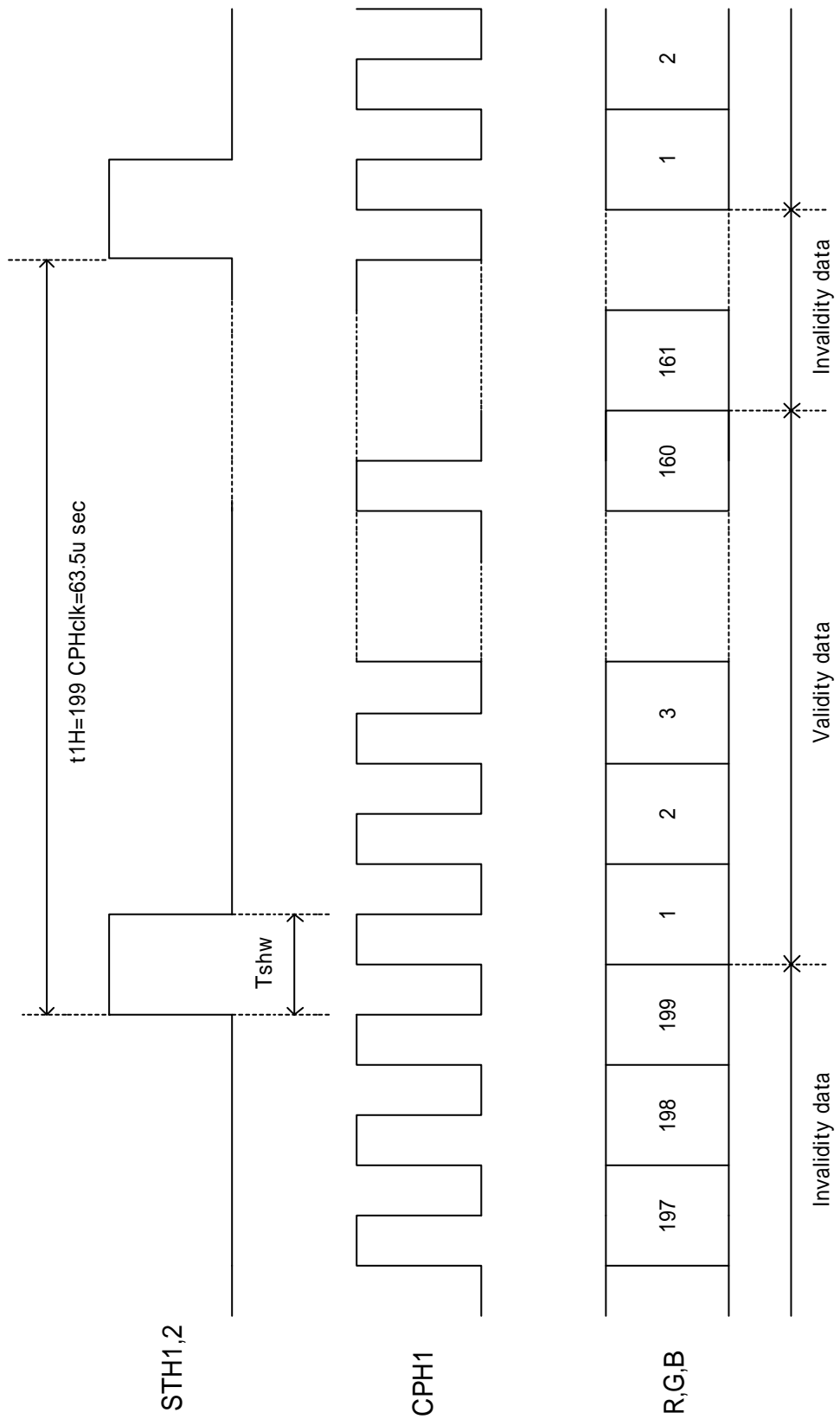


Fig. 2-1 Vertical Start Line for PAL

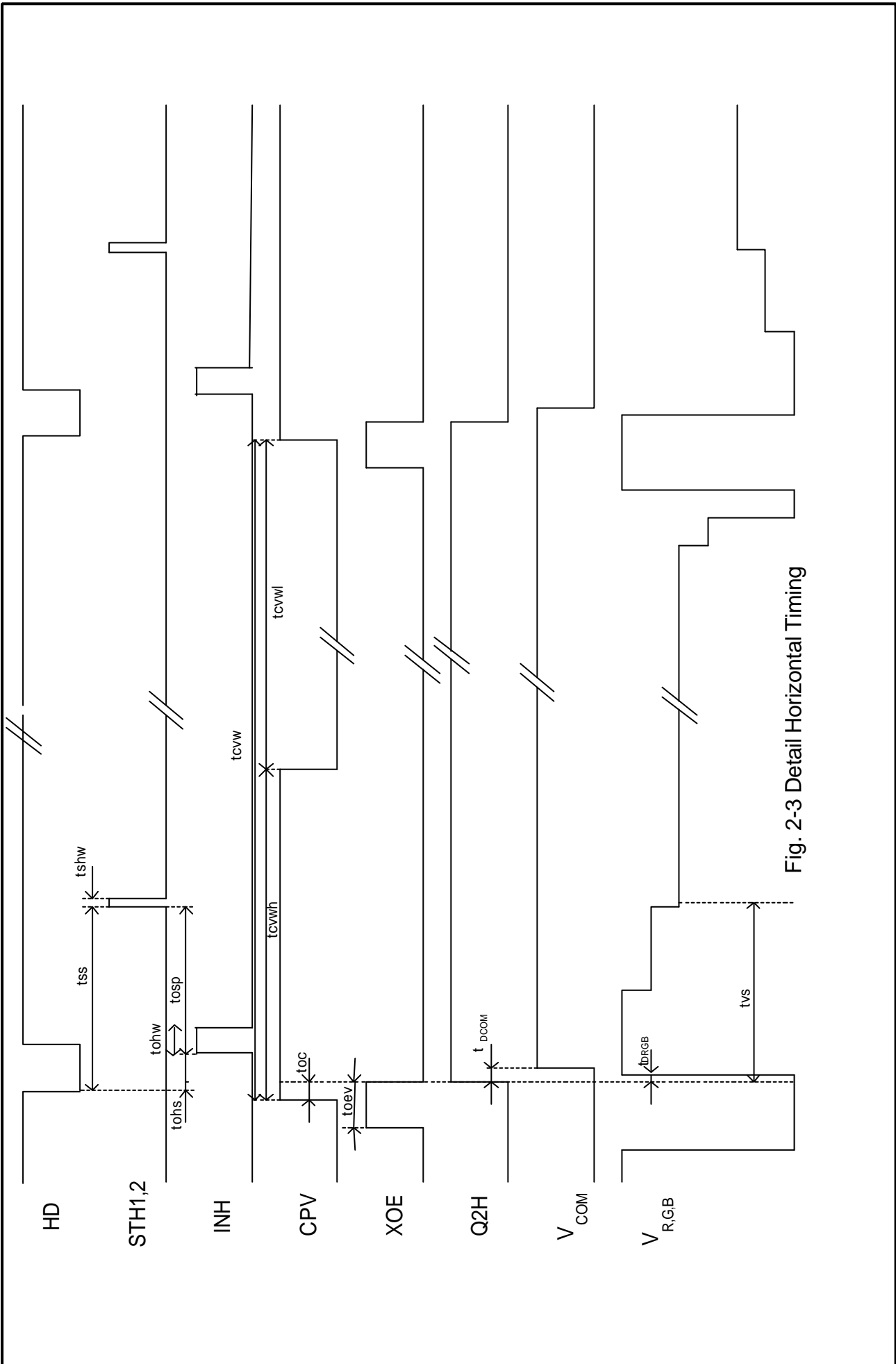


Fig. 2-3 Detail Horizontal Timing

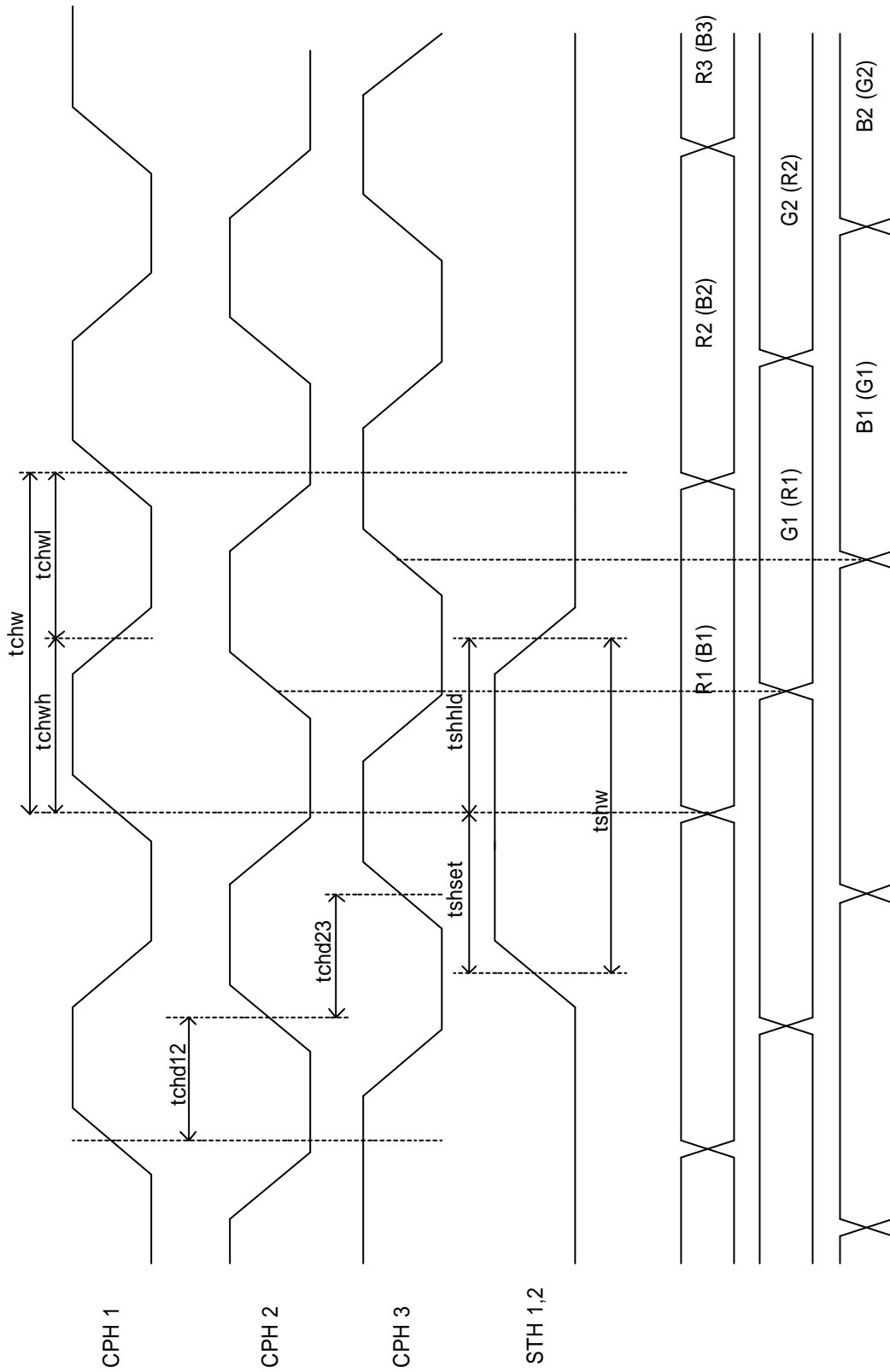


Fig. 2-4 Sampling Clock Timing

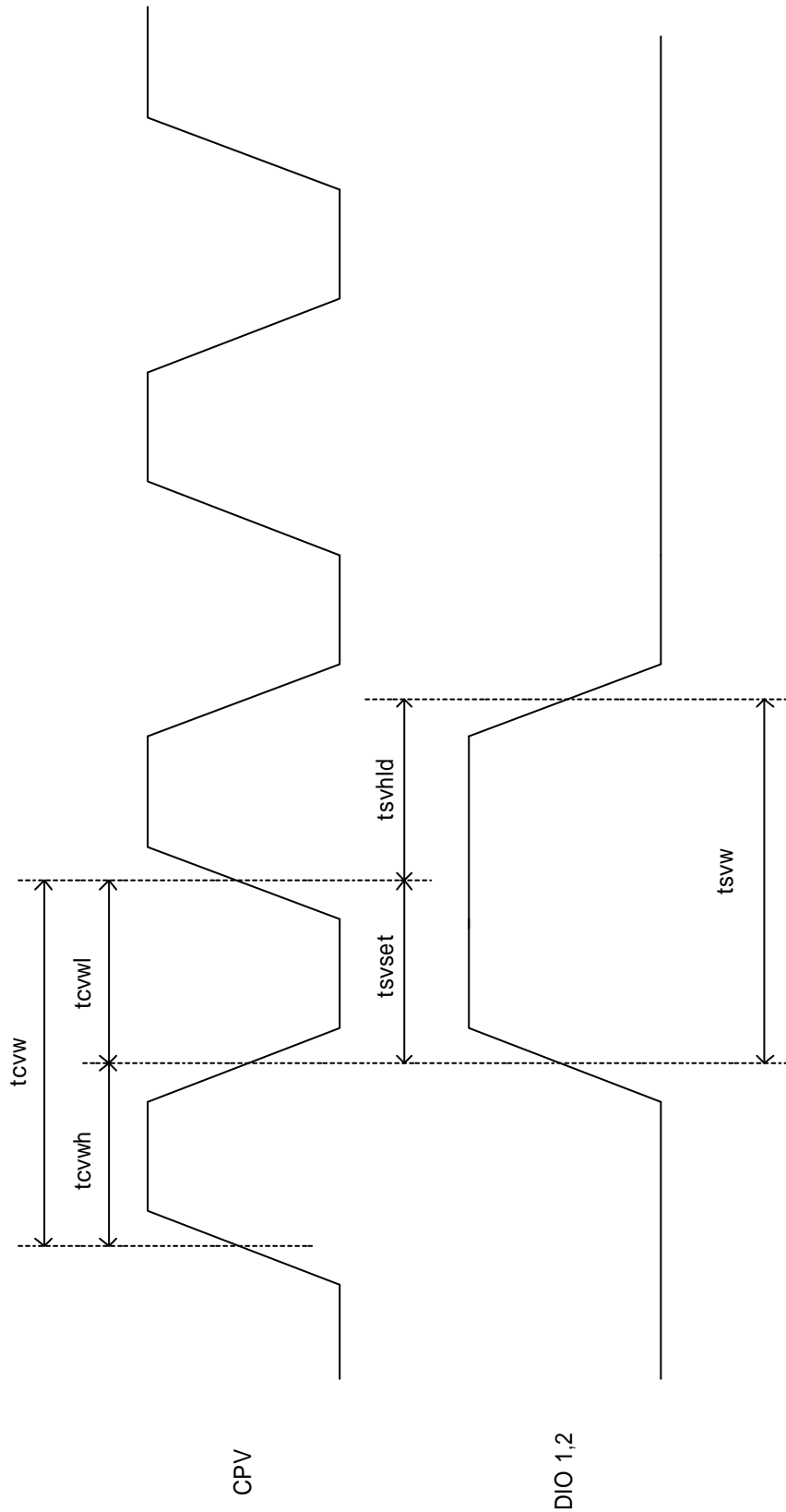


Fig. 2-5 Vertical Shift Clock Timing

Vertical timing (From up to down)

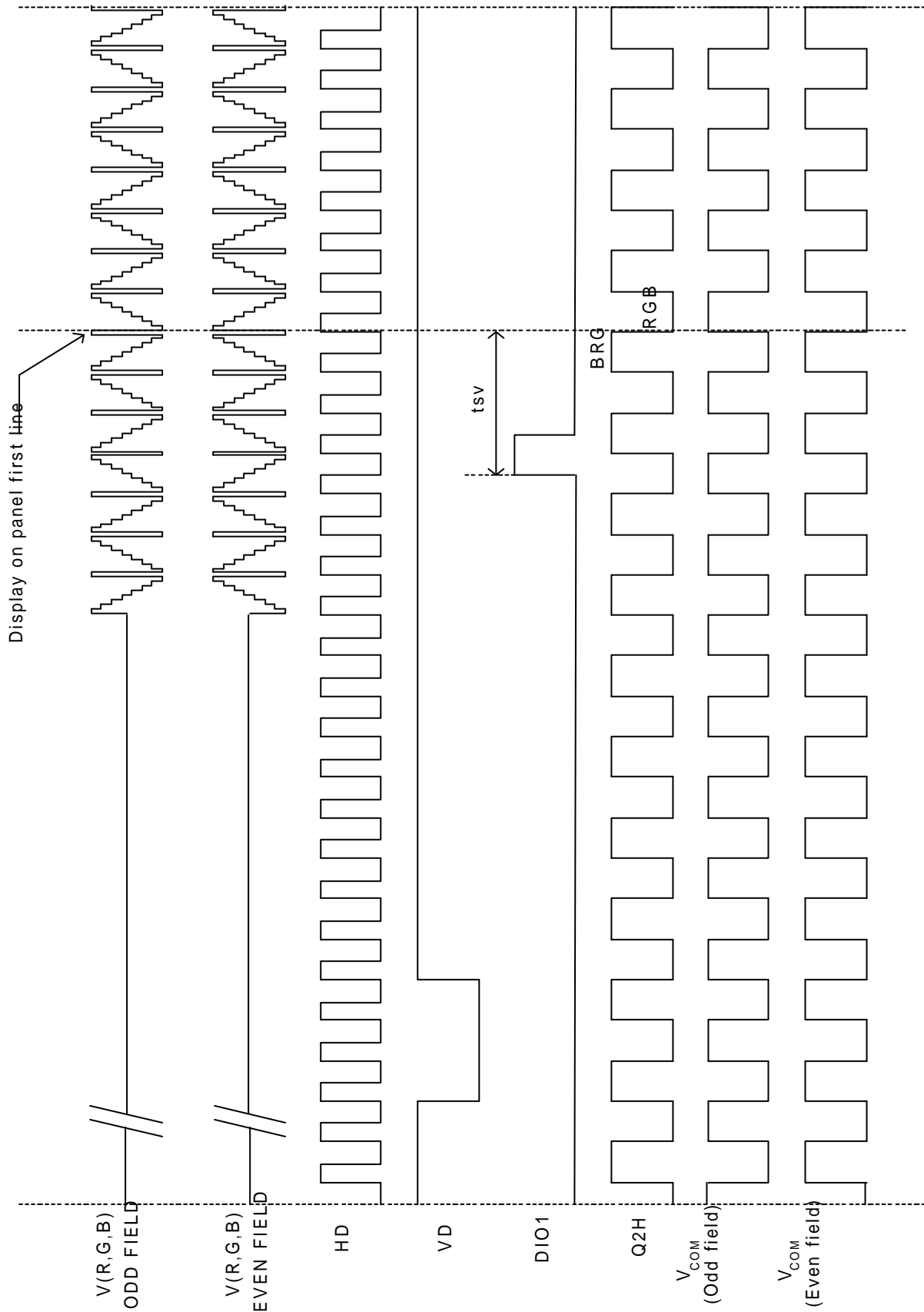


Fig.2-6 Vertical Timing (From Up to Down)

Vertical timing (From down to up)

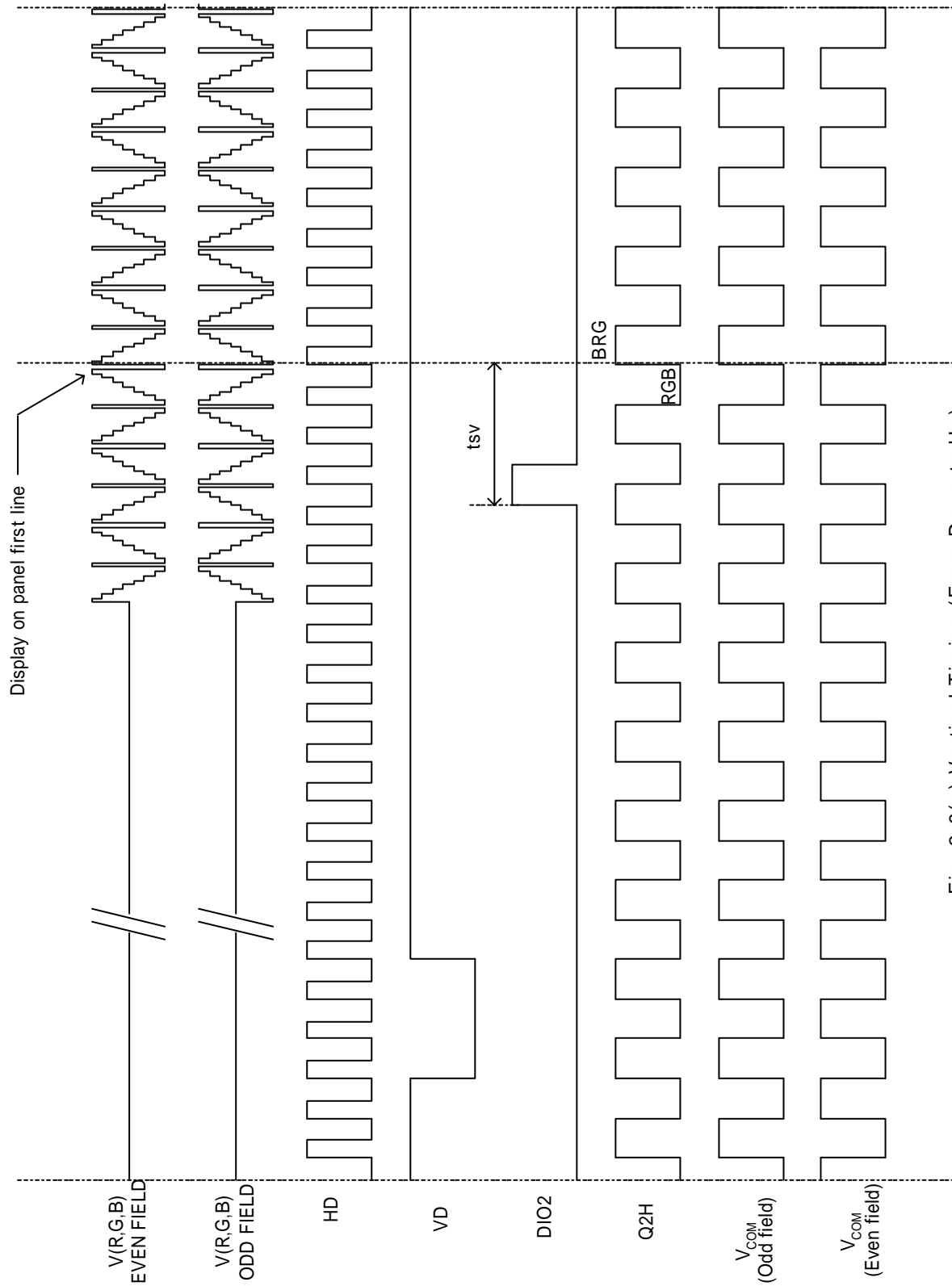
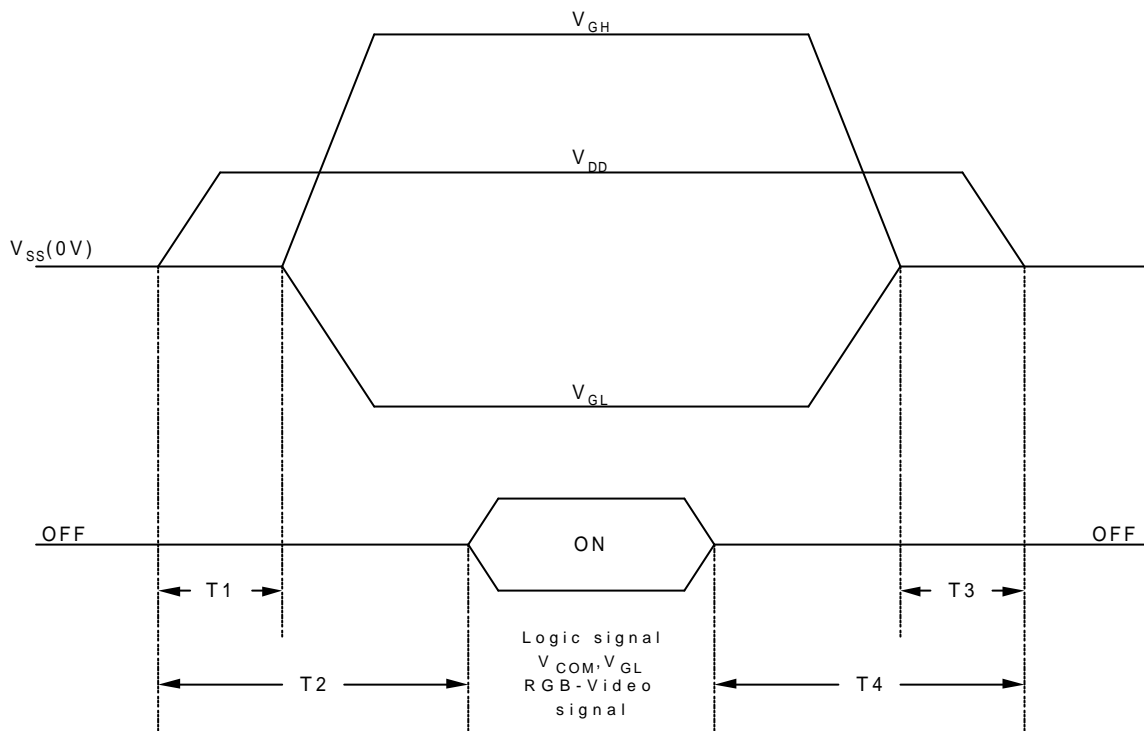


Fig. 2-6(a) Vertical Timing (From Down to Up)

2.8. Power on Sequence(Voltage source)

The Power on Sequence only effect by V_{SS} , V_{DD} and V_{GH} , the others do not care.



1) $0ms \leq T1 \leq T2$

2) $0ms < T3 \leq T4 \leq 50ms$

3. Optical Specification

3.1. Specification

Ta = 25°C

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR \geq 10	± 45	± 50		deg	Note 3-3
	Vertical	θ (to 12 o'clock)		10	15		deg	
		θ (to 6 o'clock)		30	35		deg	
Contrast Ratio		CR	At optimized Viewing angle	110	150			Note 3-1
Response time	Rise	Tr	$\theta=0^\circ$		15	30	ms	Note 3-4
	Fall	Tf	$\phi=0^\circ$		25	50	ms	
Reflectance	Ratio	R			(2.0)		%	
Transmission	Ratio	T			(8.0)		%	
White Chromaticity	x		$\theta=0^\circ$	(0.263)	(0.313)	(0.363)		Note 3-2
	y			(0.291)	(0.341)	(0.391)		

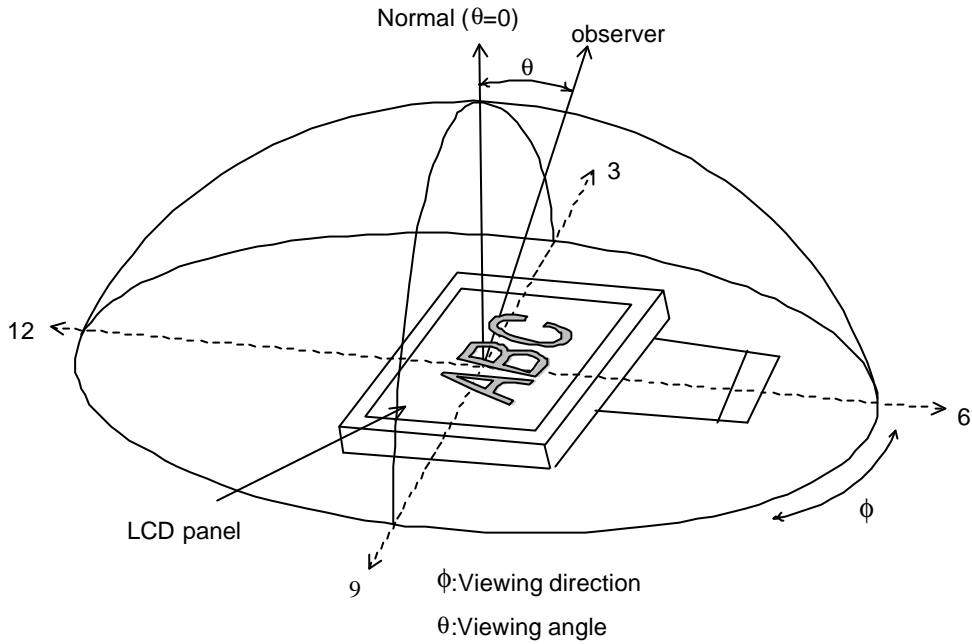
Note 3-1 : CR = $\frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

Contrast Ratio is measured in optimum common electrode voltage.

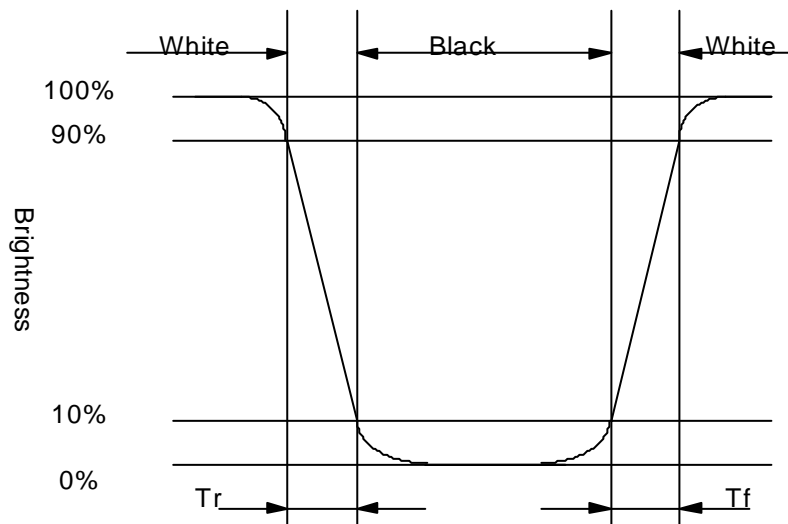
The test configurations of contrast ratio see section 3-2.

- Note 3-2: 1.Topcon BM-7(fast) luminance meter 1.0°field of view is used in the testing (use specified backlight after 20~30 minutes operation).
 2.Lamp current: 3 mA
 3.Inverter model: TDK-347.
 4.Backlight Module: 13-0250041

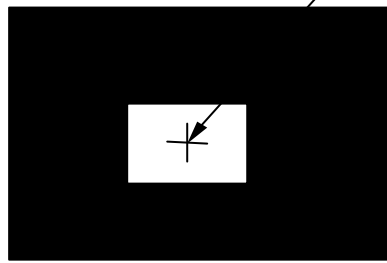
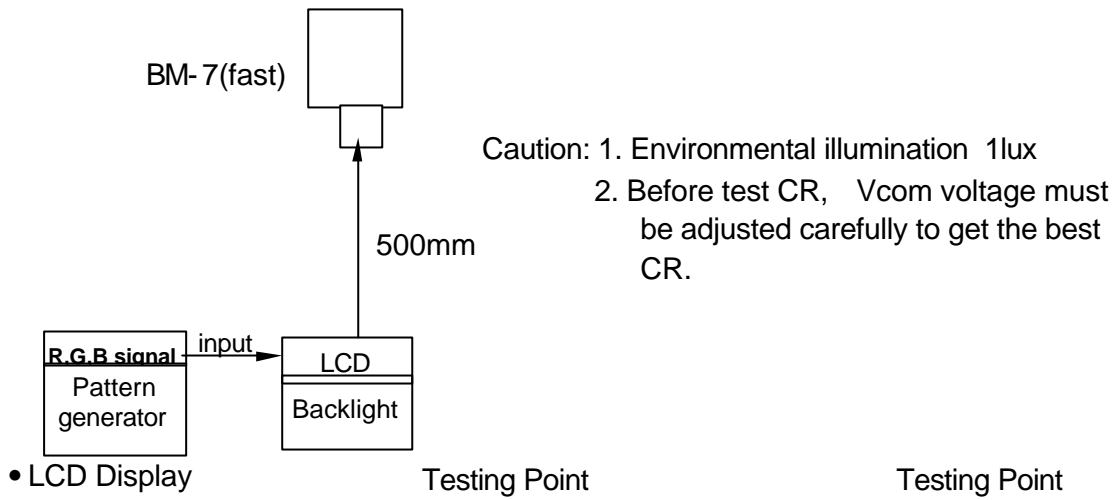
Note 3-3: The definition of viewing angle diagrams :



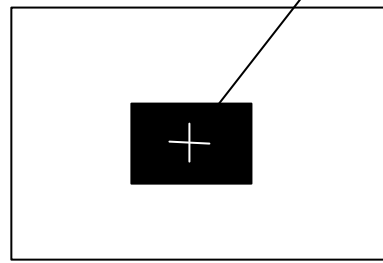
Note 3-4: The definitions of response time:



3.2. Test Configuration(Tentative)

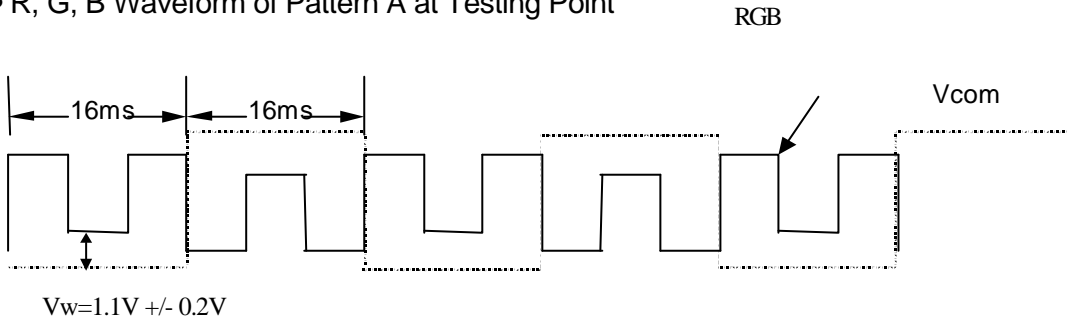


Pattern A

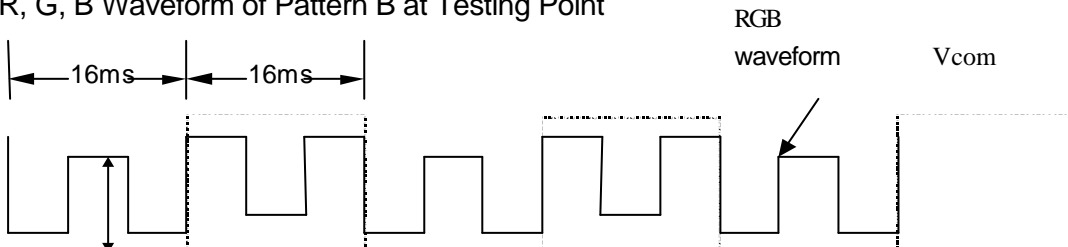


Pattern B

• R, G, B Waveform of Pattern A at Testing Point



• R, G, B Waveform of Pattern B at Testing Point



4.I/O Terminal

4.1.Pin Assignment

Pin No	Symbol	I/O	Description	Remark
1	STH1	I/O	Start pulse for source driver	Note 4-1
2	INH	I	Output enable for source driver	
3	Q2H	I	Video input rotation control	
4	CPH1	I	Sampling and shift clock for source driver	
5	CPH2	I	Sampling and shift clock for source driver	
6	CPH3	I	Sampling and shift clock for source driver	
7	V _{SS}	I	GND	
8	V _B	I	Video Input B	Note 4-4
9	V _G	I	Video Input G	
10	V _R	I	Video Input R	
11	NC	-	No connection	
12	R/L	I	Left/Right Control for source driver	Note 4-1
13	STH2	I/O	Start pulse for source driver	Note 4-1
14	AV _{DD}	I	Analog power input for source driver	Note 4-2
15	V _{COM}	I	Common electrode voltage	Note 4-4
16	V _{GH}	I	Gate on voltage	Note 4-6
17	V _{DD}	I	Digital power input	Note 4-3
18	DIO2	I/O	Vertical start pulse	Note 4-5
19	XOE	I	Output enable for gate driver	
20	CPV	I	Clock input for gate driver	
21	U/D	I	Up/Down Control for gate driver	Note 4-5
22	DIO1	I/O	Vertical start pulse	
23	NC	-	No connection	
24	V _{GL}	I	Gate off voltage(alternative every 1-H)	Note 4-4

Note 4-1 : STH1, STH2 and R/L mode

R/L	STH1	STH2	Remark
High (VDD)	Input	Output	Left to Right
Low (0 Volt.)	Output	Input	Right to Left

Note 4-2 : AV_{DD} = +5V (Typ.)

Note 4-3 : V_{DD} = +5V (Typ.)

Note 4-4 : V_{COM} = 5V_{PP}.

Phase of the video signal input and V_{COM}
 The relation between these values could refer to 5-1 Operating condition.

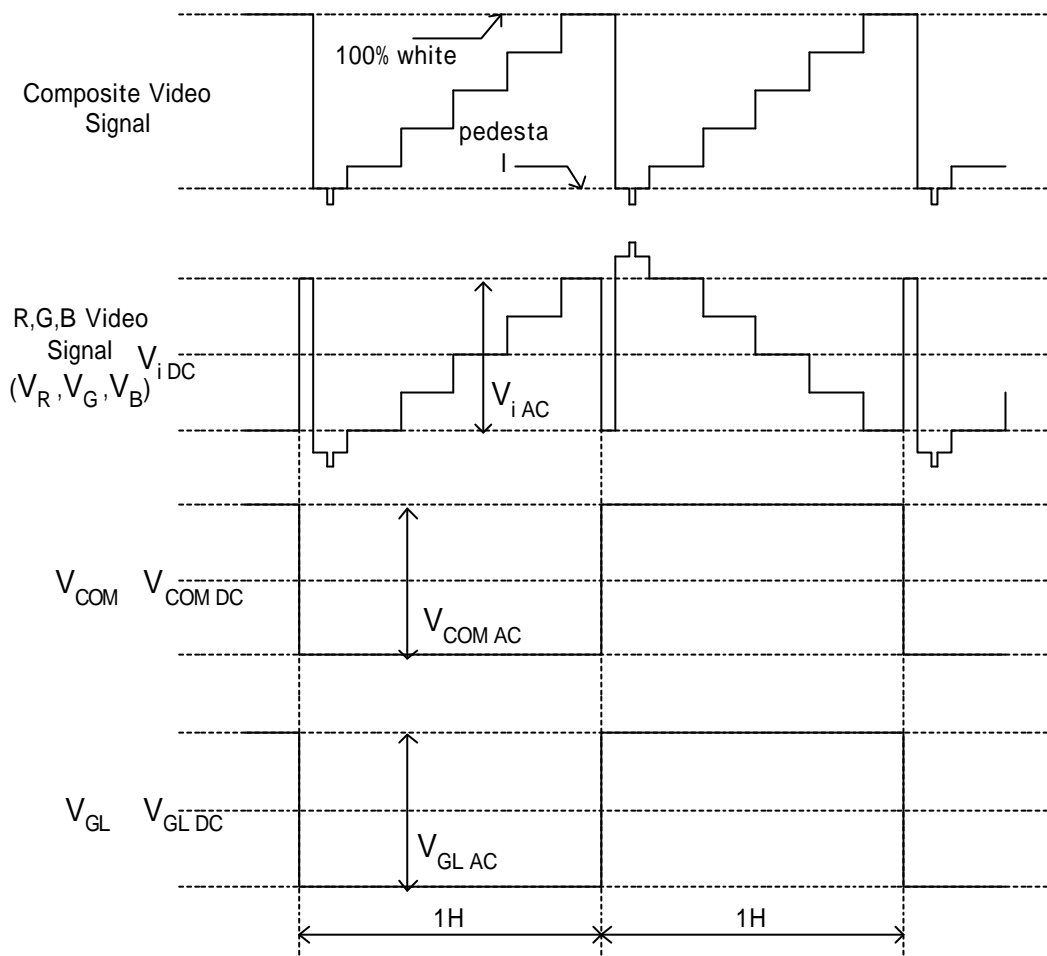


Fig.1

Liquid crystal transmission of the video signal input , V_{COM} and timing

	V_{COM}	
	H Level	L Level
Video Signal Input Maximum	Black	White
Video Signal Input Minimum	White	Black

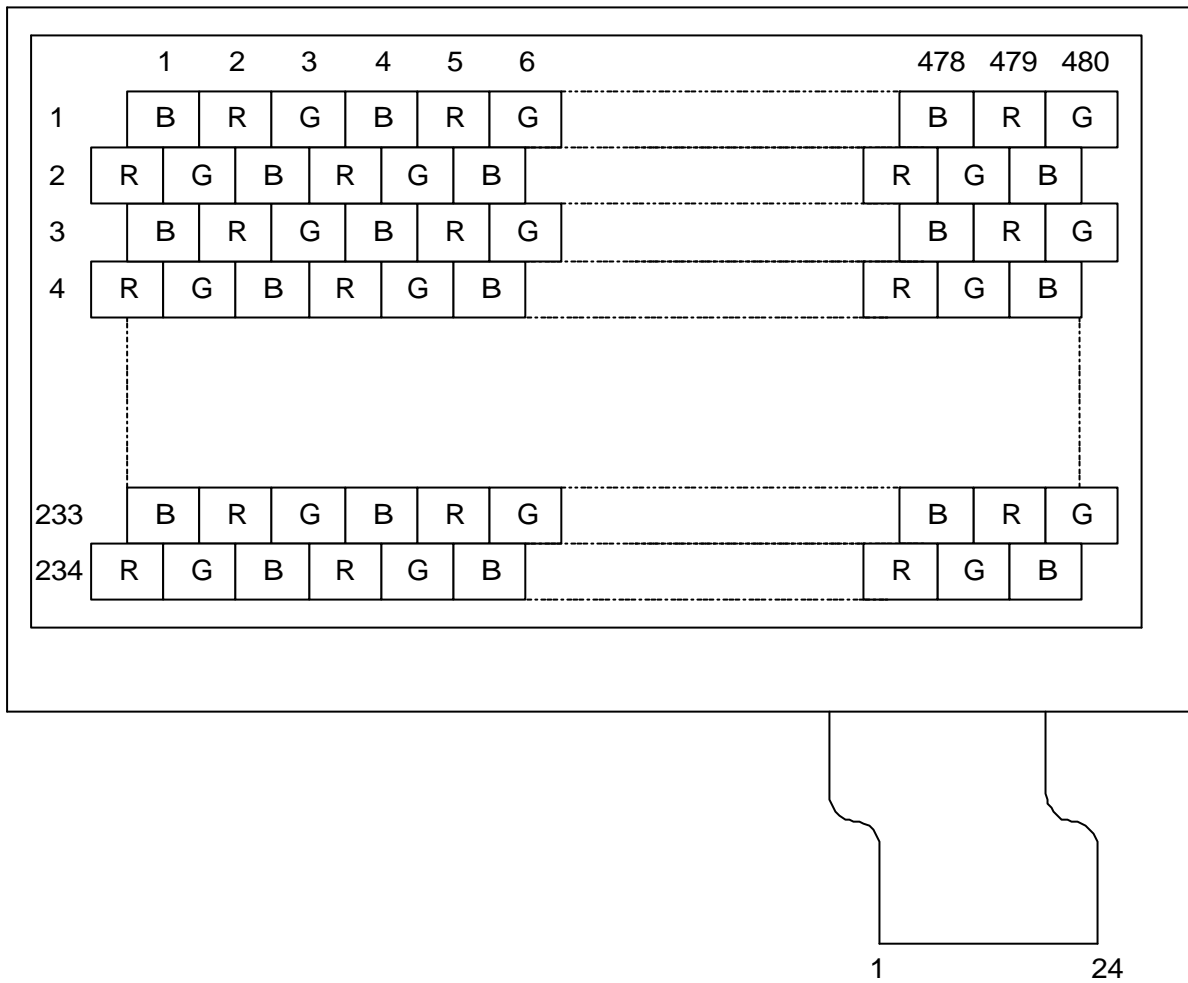
White: maximum transmission / Black: minimum transmission

Note 4-5: DIO1, DIO2 and U/D mode

U/D	DIO1	DIO2	Remark
High (VDD)	Input	Output	Down to Up
Low (0 Volt.)	Output	Input	Up to Down

Note 4-6: $V_{GH} = +15V$ (Typ.)

4.2. Pixel Arrangement and input connector pin NO.



5. Test

No change on display and in operation under the following test condition.

Conditions: Unless otherwise specified, tests will be conducted under the following condition.

Temperature : $20 \pm 5^\circ$

Humidity : $65 \pm 5\%RH$

Tests will be not conducted under functioning state.

No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70°C, 96 hrs(operation state)
2	Low Temperature Storage Test	Ta = -20°C, 96 hrs(operation state)
3	High Temperature Operation Test	Ta = 5°C, 96 hrs(operation state)
3	Low Temperature Operation Test	Ta = 0°C, 96 hrs(operation state)
4	High Humidity Test	Ta = +40°C, 90%RH, 96 hrs(operation state)
5	Thermal Cycling Test	-20°C → +25°C → +70°C, 10 Cycles 30 min 5min 30 min
6	Vibration Test	Frequency: 10 ~ 57 Hz Half Amplitude: 0.075 mm 57 ~ 500Hz: 9.8/s ² peak Cycles: 11min 3 hour (direction of X, Y, Z for 1 hour)
7	ESD Test	Voltage the stamp passable to each terminal. Condition : Machine model(MIL test method) Stamp passable voltage : 200V Capacity : 200pF Electric discharge resistance: 0Ω Stamp passable point : LCD center(1 point)
8	Shock Test	490m/s ² 11msec half-sinepulse One cycle to 3 directions of X, Y, Z

Ta: ambient temperature

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

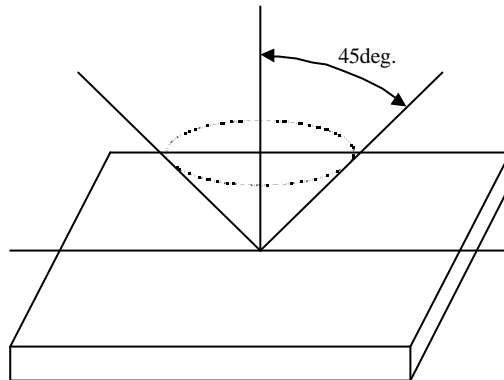
6. Appearance Standards

6.1. Inspection Conditions

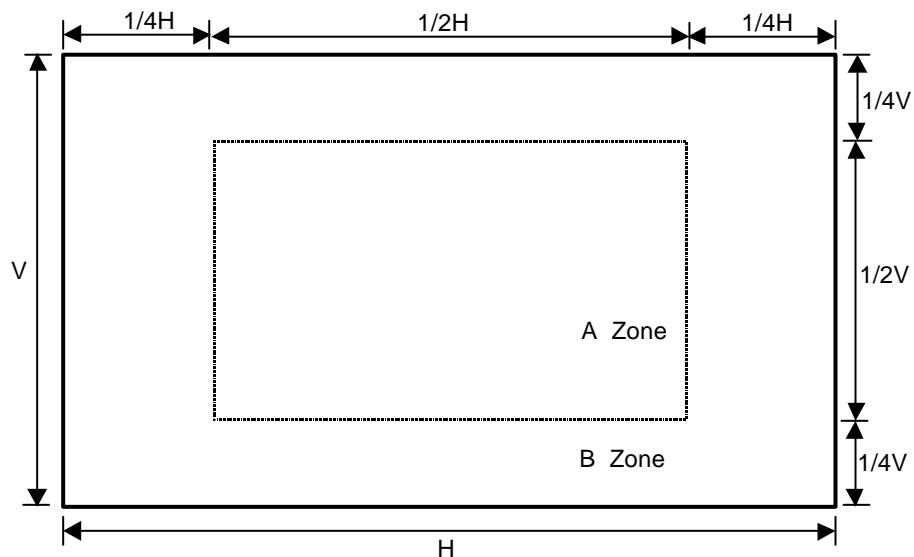
The LCD shall be inspected under 20W white fluorescent light.

The distance between the eyes and the sample shall be more than 30cm.

All directions for inspecting the sample should be 45deg. from normal to the surface.



6.2. Definition of Applied Zones



X : Maximum Seal Line

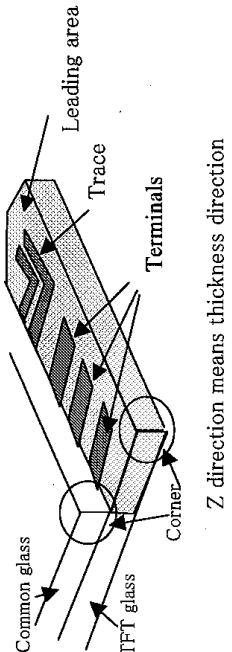
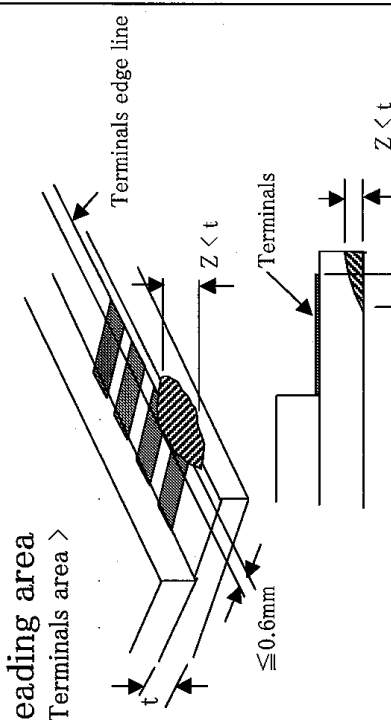
Note1. Dot Defect is Defined That the Defective Area of the Dot is Larger Than 50% of the Dot Area.

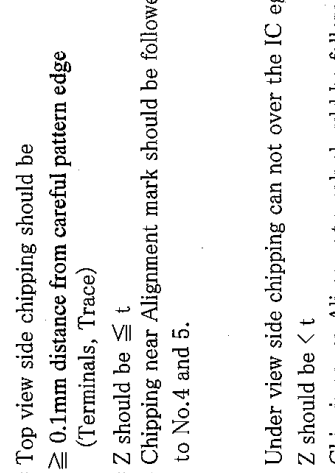
Note2. The Distance Between the Dot Defect Should be More Than 5mm Part.

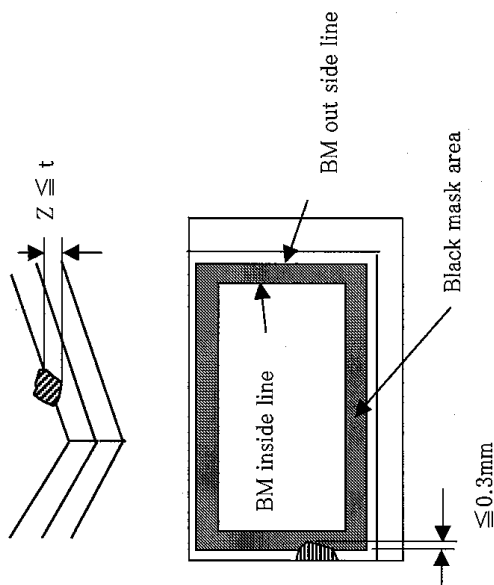
6.3. Standards

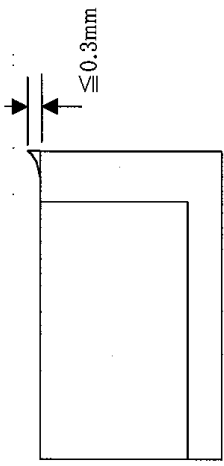
Item		Specification/Description			Classification	Note	
Display	Function	No Display			Major		
		Malfunction					
Inspection (operation)	Contrast ratio (Black,White)	Out of Spec			Major		
	Line defect	No obvious Vertical and Horizontal line defect in bright, dark and colored			Major		
	Point defect (1dot)	Area			Major	9.2	
		Item	A	B			Total
		Bright	0	3			7
Dark		1	3				
2 or more pixels in adjacent are not allowed							
External Inspection	Scratch on the polarizeer	N=3max (W≤0.1or L≤2.0) N=0 (W>0.1orL>2.0)			Major		
	Dent or Bubble on the polarizeer	N=3max(D≤0.3) N disregard(D≤0.05)			Major		
	Foreign material on the polarizeer	N=2max(D≤0.5) N disregard(D≤0.1)			Major		
	Crack	No obvious in display area			Minor		
	Chipping	No obvious in display area			Minor		
	Scratch on the Glass	No obvious in display area			Major		

Note: Minor Defect that will not result in functioning problem with deviation as classified.

Drawing	NO.	Specifications	Remark
<p>The definition of LCD part name</p>  <p>Z direction means thickness direction</p>	<p>1</p>	<p>* The maximum length can not over 0.6 mm from terminals edge line.</p> <p>* Z should be $< t$</p>	
<p>Leading area < Terminals area ></p> 			

Drawing	NO.	Specifications	Remark
<p data-bbox="327 324 359 492">< Un-Terminals area ></p>  <p data-bbox="383 537 414 694">Top view</p> <p data-bbox="383 806 414 1008">Careful pattern (Terminals, Trace)</p> <p data-bbox="383 1075 414 1232">Under view</p>	<p data-bbox="327 1019 351 1052">2</p> <p data-bbox="327 1590 351 1624">3</p>	<p data-bbox="327 1590 718 1830">* Top view side chipping should be $\geq 0.1\text{mm}$ distance from careful pattern edge (Terminals, Trace) * Z should be $\leq t$ * Chipping near Alignment mark should be followed to No.4 and 5.</p> <p data-bbox="718 1590 1133 1830">* Under view side chipping can not over the IC edge line * Z should be $< t$ * Chipping near Alignment mark should be followed to No.4 and 5.</p>	

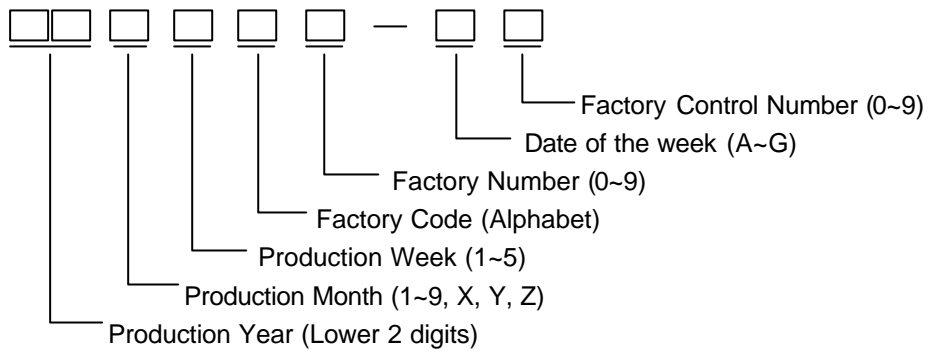
Drawing	NO.	Remark
<p data-bbox="359 504 399 716">Un-Leading area</p> 	<p data-bbox="406 1041 430 1064">6</p> <p data-bbox="406 571 566 1008">* Chipping start from black mask outside line to inside line ≤ 0.3 mm Z should be $\leq t$</p>	

Drawing	NO.	Specifications	Remark
<p>Jutting</p> 	7	<p>Jutting ≤ 0.3 mm Applied for all corner of TFT glass and Common glas</p>	

Rev: 002 02.22.2002 製張 名 panel-opt

7.Code System of Production Lot

The production lot of module is specified as follows.



8.Type Number

The type number of module is specified as follows.

51654AE

9.Applying Precautions

Please contact us when questions and/or new problems not specified in this Specifications arise.

10. Precautions Relating Product Handling

The Following precautions will guide you in handling our product correctly.

- 1) Liquid crystal display devices
 1. The liquid crystal display device panel used in the liquid crystal display module is made of plate glass. Avoid any strong mechanical shock. Should the glass break handle it with care.
 2. The polarizer adhering to the surface of the LCD is made of a soft material. Guard against scratching it.
- 2) Care of the liquid crystal display module against static electricity discharge.
 1. When working with the module, be sure to ground your body and any electrical equipment you may be using. We strongly recommend the use of anti static mats (made of rubber), to protect work tables against the hazards of electrical shock.
 2. Avoid the use of work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.
 3. Slowly and carefully remove the protective film from the LCD module, since this operation can generate static electricity.
- 3) When the LCD module alone must be stored for long periods of time:
 1. Protect the modules from high temperature and humidity.
 2. Keep the modules out of direct sunlight or direct exposure to ultraviolet rays.
 3. Protect the modules from excessive external forces.
- 4) Use the module with a power supply that is equipped with an overcurrent protector circuit, since the module is not provided with this protective feature.
- 5) Do not ingest the LCD fluid itself should it leak out of a damaged LCD module. Should hands or clothing come in contact with LCD fluid, wash immediately with soap.
- 6) Conductivity is not guaranteed for models that use metal holders where solder connections between the metal holder and the PCB are not used. Please contact us to discuss appropriate ways to assure conductivity.
- 7) For models which use CFL:
 1. High voltage of 1000V or greater is applied to the CFL cable connector area. Care should be taken not to touch connection areas to avoid burns.
 2. Protect CFL cables from rubbing against the unit and thus causing the wire jacket to become worn.
 3. The use of CFLs for extended periods of time at low temperatures will significantly shorten their service life.
- 8) For models which use touch panels:
 1. Do not stack up modules since they can be damaged by components on neighboring modules.
 2. Do not place heavy objects on top of the product. This could cause glass breakage.
- 9) For models which use COG, TAB, or COF:
 1. The mechanical strength of the product is low since the IC chip faces out unprotected from the rear. Be sure to protect the rear of the IC chip from external forces.
 2. Given the fact that the rear of the IC chip is left exposed, in order to protect the unit from electrical damage, avoid installation configurations in which the rear of the IC chip runs the risk of making any electrical contact.

10) Models which use flexible cable, heat seal, or TAB:

1. In order to maintain reliability, do not touch or hold by the connector area.
2. Avoid any bending, pulling, or other excessive force, which can result in broken connections.

11) In case of buffer material such as cushion / gasket is assembled into LCD module, it may have an adverse effect on connecting parts (LCD panel-TCP / HEAT SEAL / FPC / etc., PCB-TCP / HEAT SEAL / FPC etc., TCP-HEAT SEAL, TCP-FPC, HEAT SEAL-FPC, etc.,) depending on its materials.

Please check and evaluate these materials carefully before use.

12) In case of acrylic plate is attached to front side of LCD panel, cloudiness (very small cracks) can occur on acrylic plate, being influenced by some components generated from polarizer film..

Please check and evaluate those acrylic materials carefully before use.

11. Warranty

This product has been manufactured to your company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. When the product is in CFL models, CFL service life and brightness will vary According to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
5. We cannot accept responsibility for intellectual property of a third party, which may arise through the application of our product to your assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.
6. Optrex will not be held responsible for any quality guarantee issue for defect products judged as Optrex-origin longer than 2 (two) years from Optrex production or 1(one) year from Optrex, Optrex America, Optrex Europe delivery which ever comes later.